Low Standby-Power Quasi-Resonant Primary-Side Converter

General Description

The PN8370 consists of a Low Standby-Power Quasi-Resonant (QR) Primary-Side controller and a 650V avalanche-rugged smart power VDMOSFET, specifically designed for a high performance AC/DC charger or adaptor with minimal external components. PN8370 operates in primary-side sensing and regulation, so opto-coupler and TL431 could be eliminated. Because of internal HV Start-up circuit, the system with PN8370 can achieve less than 30mW standby power consumption (230VAC). In CV mode, multi-mode and quasi resonant technique is utilized to achieve high efficiency, avoid audible noise and make the system meeting Energy star class VI. Good load regulation is achieved by the built-in cable drop compensation. In CC mode, the current and output power setting can be adjusted externally by the sense resistor at CS pin. PN8370 offers complete protections including Cycle-by-Cycle current limiting protection (OCP), over voltage protection (OVP), over temperature protection (OTP) and CS open or short protection (CSO/SP) etc.

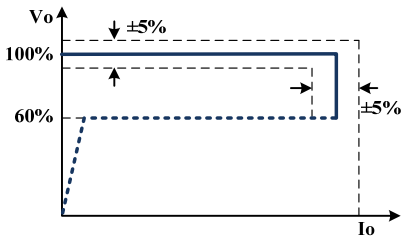
Applications

- Switch AC/DC Adaptor
- Battery Charger

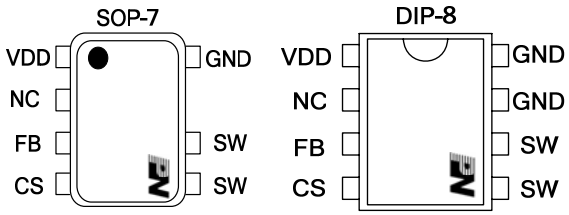
Features

- Internal 650 V avalanche-rugged smart power VDMOSFET
- Internal HV Start-up Circuit, Standby power consumption < 30mW at 230VAC
- Multi-mode and Quasi-Resonant technique achieve high efficiency, meeting energy star class VI
- ±5% CC Regulation at Universal AC input
- Primary-side Sensing and Regulation without TL431 and Opto-coupler
- Programmable Cable Drop Compensation
- No-need Control Loop Compensation Capacitance
- Excellent Protection Coverage:
  - ✧ Over Temperature Protection (OTP)
  - ✧ VDD Under/Over Voltage Protection(UVLO&OVP)
  - ✧ Cycle-by-Cycle Current Limiting (OCP)
  - ✧ Cs Short/Open Protection (CS O/SP)

Output Features

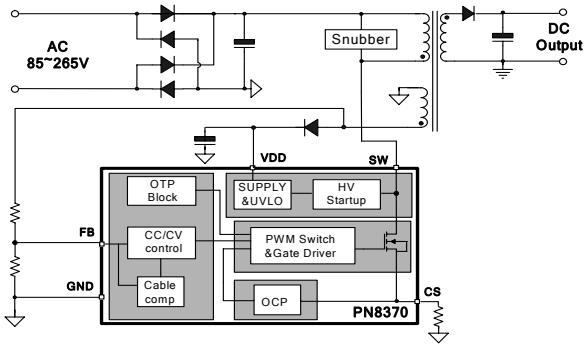


Package/Order Information



Order codes	Package	Typical power
		85~265 V_{AC}
PN8370SSC-R1	**SOP7**	**12W**
PN8370NEC-T1	**DIP8**	**15W**

Typical Application



Pin Definitions

Table 1. Pin Definitions

SOP-7 Pin Number	DIP-8 Pin Number	Pin Name	Pin Function Description
1	1	VDD	Power supply
2	2	NC	No connection
3	3	FB	The voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage.
4	4	CS	Current Sense Input
5,6	5,6	SW	Avalanche-rugged power MOSFET Drain pin. The Drain pin is connected to the primary lead of the transformer.
7	7,8	GND	Ground

Typical power

Table 2. Typical power

Part Number	**Package**	**Adapter(1)**
		85-265 V_{AC}
PN8370	**SOP-7**	**12W**
	DIP-8	**15W**

Note:

1. Maximum output power is tested in an adapter at 45°C ambient temperature, with enough cooling conditions.

Absolute Maximum Ratings

Supply voltage Pin VDD……-0.3~40V

High-Voltage Pin, SW……650V

Pin FB, CS……-0.3~5.5V

Operating Junction Temperature……-40~150℃

Storage Temperature Range……-55~150℃

Package Thermal Temperature (SOP-7) ……80°C/W

Package Thermal Temperature (DIP-8) ……40°C/W

Lead Temperature (Soldering, 10Secs)……260℃

ESD Protection (HBM, ESDA/JEDEC JDS-001-2014)……±4.0kV

Pulse Drain Current……3.0A

Electrical Characteristics

Table 3. Power section (T_J=25°C, V_{DD} = 21 V; unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{BVDSS}	Break-down voltage	I_{SW} = 250uA	650	700		V
I_{OFF}	Off-state drain current	V_{SW} = 500V			100	uA
$R_{DS(on)}$	Drain-source on state resistance	I_{SW} = 1A, T_J = 25℃		2.5		Ω
V_{SW_START}	Start up threshold	V_{DD}=V_{DDon} - 1V		30		V

Table 4. Supply section (T_J=25°C, V_{DD} = 21 V; unless otherwise specified)

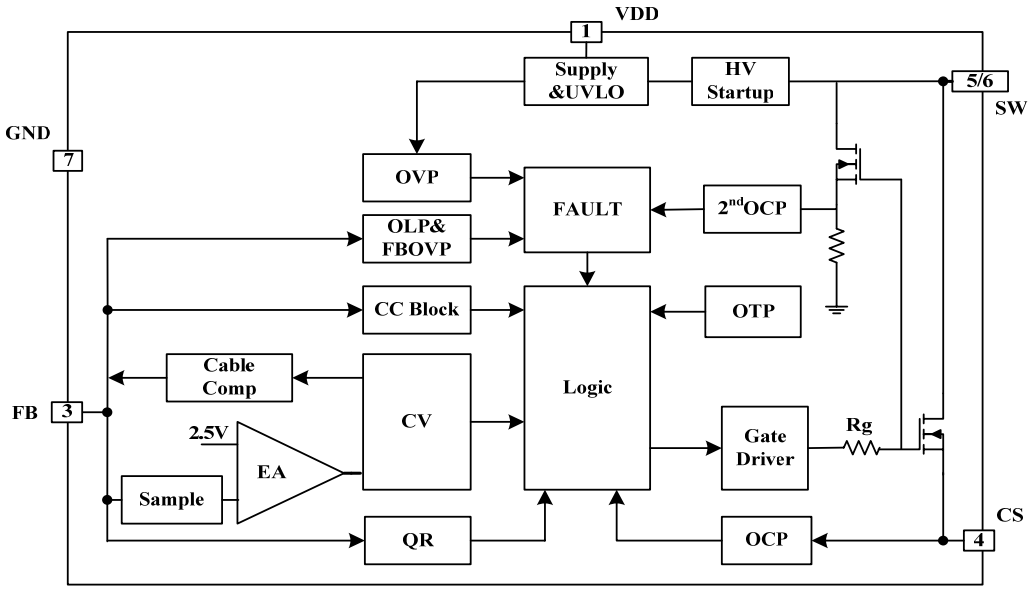
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage Section						
V_{DD}	Operating voltage range		8		30	V
V_{DDon}	VDD start up threshold		14.5	16.5	18.5	V
V_{DDoff}	VDD under voltage shutdown threshold		7.5	8.5	9.5	V
V_{DDovp}	VDD over voltage protect		30	34	38	V
Supply Current Section						
I_{DD0_CH}	VDD charge current	V_{DD}=V_{DDon} - 1V, Vsw=100V		1.5		mA
I_{DD}	Operating current, switching	V_{DD} = V_{DDon} ＋1V		0.5		mA
I_{DD_FAULT}	Operating current after fault	V_{DD}＝15V after fault		0.5		mA

Table 5. Controller section (T_J = 25°C, V_{DD} = 21 V; unless otherwise specified)

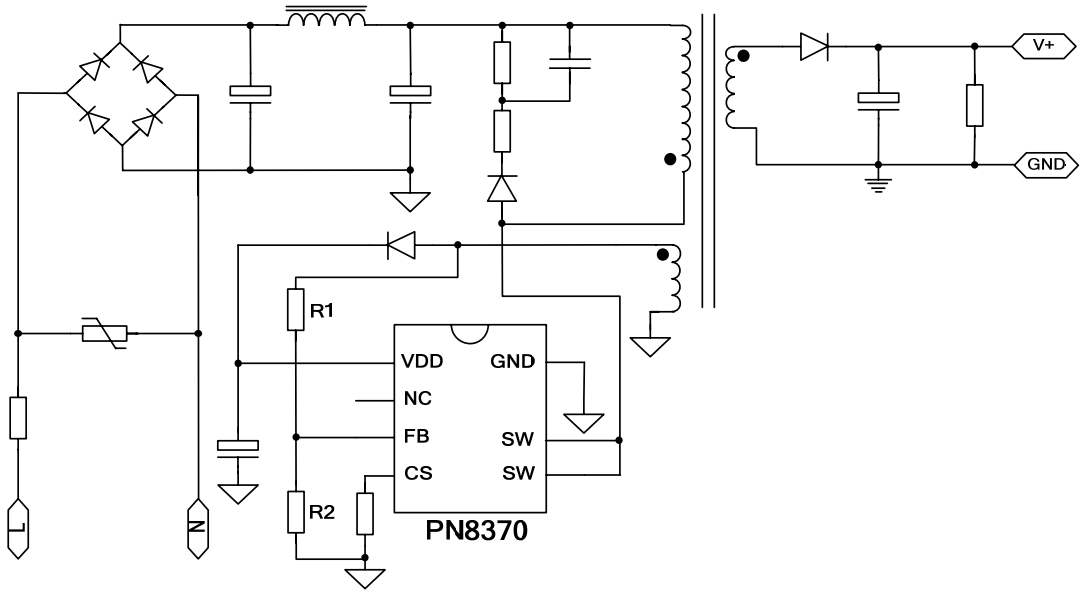
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Current Sense Section						
V_{TH_OC}	Current sense threshold		485	500	515	mV
$V_{TH\_OC\_MAX}$	Maximum Current sense threshold			550		mV
Vcs_min	Minimum CS threshold			170		mV
T_{LEB}	Leading Edge Blanking time			300		ns
T_{onmax}	Maximum Ton			50		us
T_{D_OC}	OCP propagation delay			100		ns
FB Section						
V_{REF_CV}	Reference voltage for feedback threshold		2.475	2.5	2.525	V
V_{FBOVP}	Output over voltage protection threshold		2.85	3	3.15	V
V_{UVP}	Output under voltage threshold			1.55		V
Icable	Maximum cable compensation current	V_{FB}=0V	22	24	26	uA

T_{offmin}	Minimum Toff			5		us
T_{offmax}	Maximum Toff			2.2		ms
T_{UVP}	Output under voltage protection Blanking time	F_{SW}= 50kHz	20		32	ms
THERMAL SECTION						
T_{SD}	Thermal shutdown temperature threshold		140	160		°C
T_{HYST}	Thermal shutdown hysteresis			30		°C

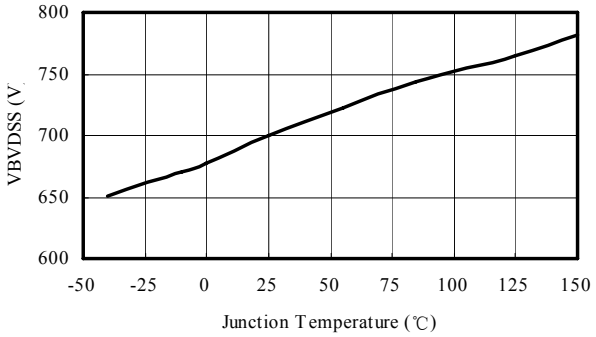
Block Diagram



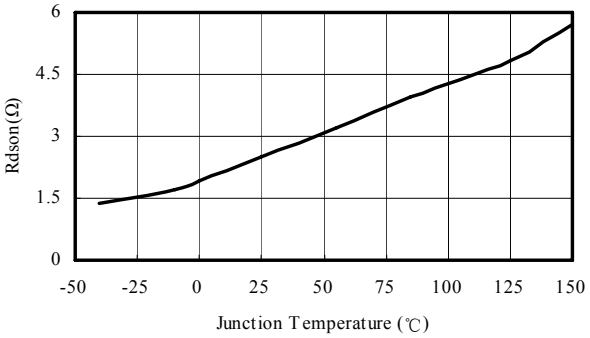
Typical Application



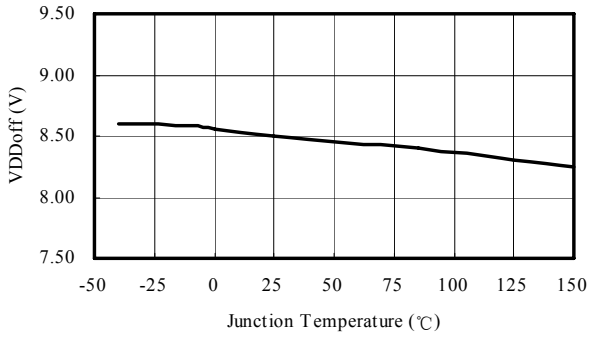
Typical Characteristics Plots



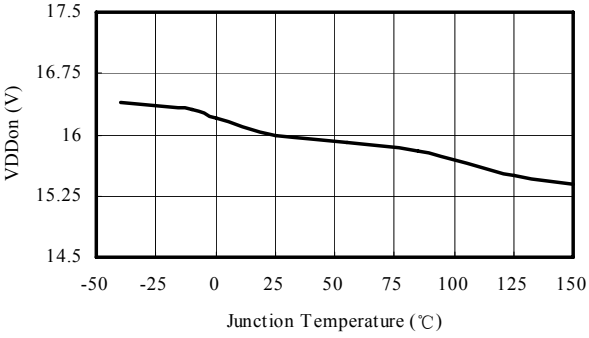
(a) BV vs Tj



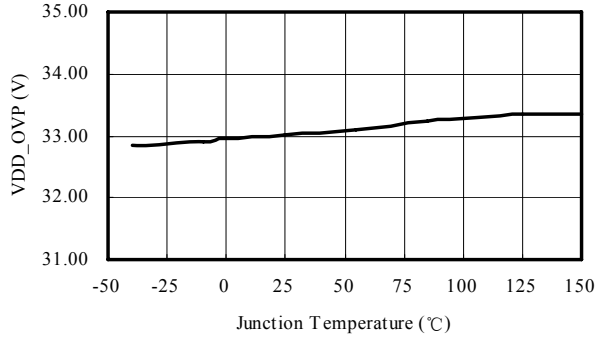
(b) Rdson vs Tj



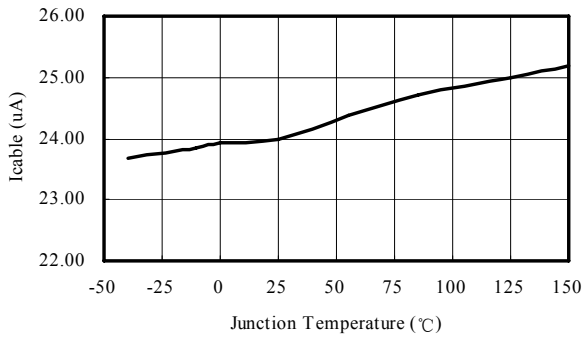
(c) V_{DDoff} vs Tj



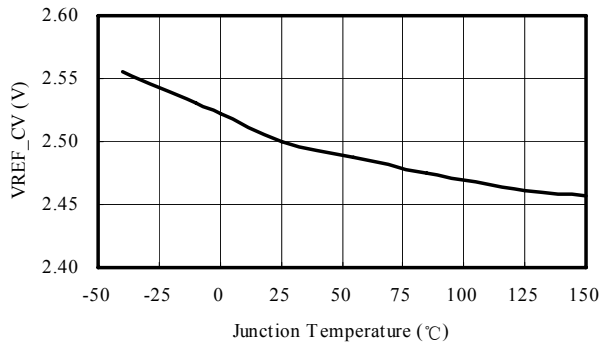
(d) V_{DDon} vs Tj



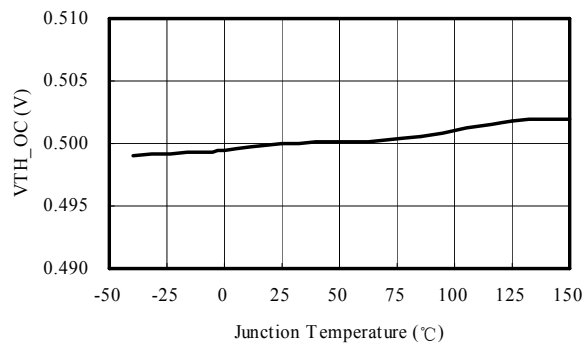
(e) VDD_OVP vs Tj



(f) Icable vs Tj



(g) V_{REF_CV} vs Tj



(h) V_{TH_OC} vs Tj

Functional Description

The PN8370 is a high performance CC/CV primary-side controller. PN8370 operates in primary-side sensing and regulation, so opto-coupler and TL431 could be eliminated. Proprietary built-in CV and CC control can achieve high precision CC/CV control meeting most charger and adaptor application requirements. Internal HV Start-up circuit and the chip's low consumption help the system to meet strict standby power standard.

1. HV Start up Control

At start up, the internal high-voltage start-up circuit provides the internal bias and charges the external VDD capacitor, so that PN8370 starts up quickly. When VDD reaches V_{DDon}, the device starts switching and the internal high-voltage current source stops charging the capacitor. The device keeps in normal operation provided as long as VDD keeps above V_{DDoff}. After startup, the bias is supplied from the auxiliary transformer winding, the current of HV start-up circuit is designed to be very low so that the power consumption is very low.

2. CC Operation Mode

In CC operation mode, the PN8370 captures the auxiliary flyback signal at FB pin through a resistor dividing-network. The pulse width of the auxiliary flyback signal determines the PN8370 oscillator frequency. The higher the output voltage is, the shorter the pulse width is, and the higher the chip oscillator frequency is, thus the constant output current can be achieved.

The current waveform of DCM mode is shown in Figure 1. During MOSFET turn-on time, the current in the primary winding (Ipri) ramps up. When MOSFET turns off, the energy stored in the primary winding is transferred to the secondary side, so the peak current in the secondary winding is

$$I_{sec\_pk} = I_{pri\_pk} \times N_{ps} \qquad (1)$$

The output current is

$$I_O = \frac{I_{sec\_pk}}{2} \times \frac{T_{demag}}{T_P} = \frac{1}{2} N_{PS} \frac{V_{ipk}}{R_{sense}} \frac{T_{demag}}{T_P} \qquad (2)$$

Because Vipk is constant and Tp is equal to tow times Tdemag, the output current Io is constant.

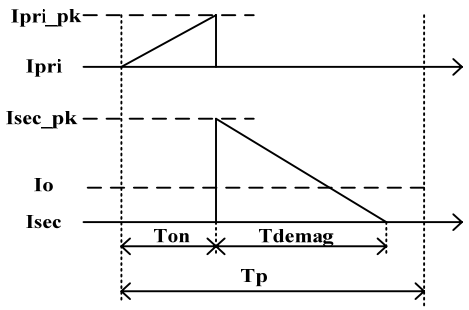


Figure 1 The current waveform of DCM mode

3. CV Operation Mode

In CV mode，PN8370 uses a pulse to sample V_{FB} and it is hold until the next sampling. The sampled voltage is compared with V_{REF_CV} and the error is amplified. The error amplified output reflects the load condition and controls the switching off time to regulate the output voltage, thus constant output voltage can be achieved.

The relationship between the output voltage and V_{REF_CV} is

$$Vo = (V_{REF\_CV} \times \frac{R1+R2}{R2}) \times \frac{N_S}{N_{AUX}} \quad (3)$$

N_S means Secondary winding, N_{AUX} means Auxiliary winding

The PN8370 operates in PFM_QR mode during full load mode, since the peak current (Ipeak) of MOSFET is constant, the chip frequency decreases while the output current decreases. When the switching frequency approaches to 25kHz, the PN8370 enters PWM_QR mode , the chip frequency decreases slowly while the output current decreases, the Ipeak decreases while the output current decreases. Therefore the PN8370 can avoid audible noise, while achieving high efficiency at 25% load conditions. When Vcs decreases to 170mV, the PN8370 enters Standby mode. In this mode, Ipeak keeps around constant, the chip oscillator frequency decreases while the output current decreases. Figure 2 illustrates the relations of the switching frequency, Ipeak and Loading for PN8370.

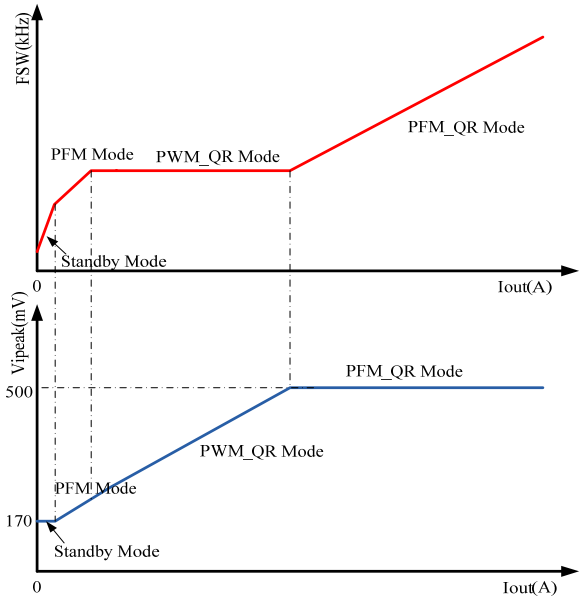


Figure 2 The Switching Frequency, Vipeak VS. LOAD

4. Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in PN8370. The switch current is detected by a sense resistor at CS pin. The CC set-point and maximum output power can be externally adjusted by external current sense resistor at CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial power MOSFET on-state so that the external RC filtering on sense input is no longer needed.

5. Programmable Cable Drop Compensation

In PN8370, an offset voltage is generated at FB pin by an internal current flowing into the divider resister, as shown in Figure 3. The Cable Drop Compensation block compensates the voltage drop across the cable. As the load current decreases from full load to no load, the voltage drop across the cable decreases. It can be programmed by adjusting the external resistor R2 or R1 at FB pin. The maximum compensation is

$$\frac{V_{cable}}{V_O} = \frac{I_{cable} \times (R2 // R1)}{2.5V} \quad (4)$$

Because of the influence of the chip's sampling position and devices of the system, the actual maximum compensation is less than theoretical value.

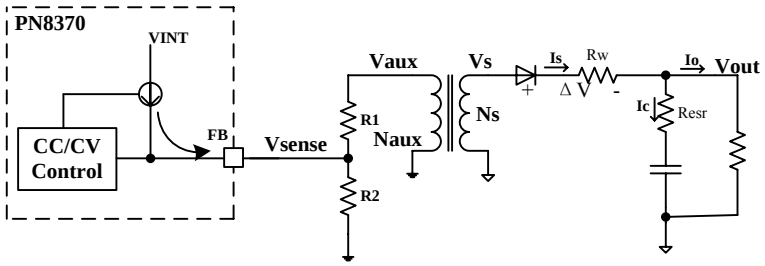


Figure 3 Icable

6. Reference Negative Temperature Compensation

As shown in Figure 3, the voltage of FB pin is

$$V_{FB} = K(V_O + \Delta V), K = \frac{R2 \times N_{AUX}}{(R1 + R2) \times N_S} \quad (5)$$

Where △V has a negative temperature coefficient, K is a constant.

In PN8370, the voltage reference uses the negative temperature compensation technology. At room temperature, the voltage reference is 2.5V. The voltage reference (V_{REF_CV}) decreases while the temperature of chip increases. The reference negative temperature compensation block compensates the △V, thus the output voltage keeps constant at full range of temperature. The reference negative temperature compensation improves output precision.

7. Quasi-Resonant Switching

The PN8370 incorporates a unique proprietary quasi-resonant switching scheme that achieves valley-mode turn on for every switching cycle in CV mode. This unique feature greatly reduces the switching loss. The actual switching frequency can vary slightly cycle by cycle, providing the additional benefit of reducing EMI.

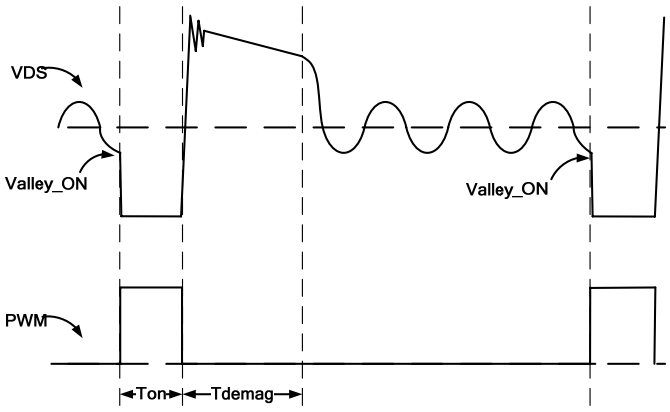


Figure 4 QR Mode

8. Protection Control

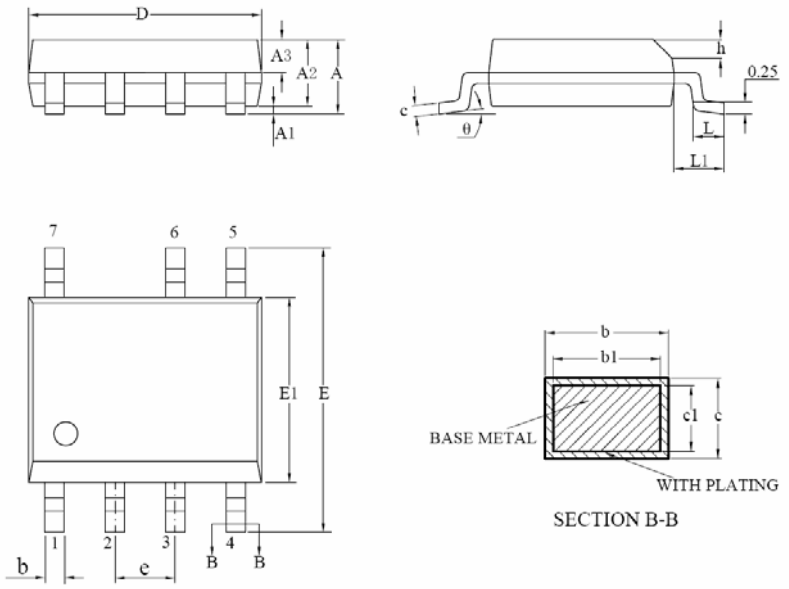
The PN8370 has several self-protection functions, such as Cycle-by-Cycle current limiting (OCP), Over-Voltage Protection, Over-Temperature Protection, Feedback Loop open Protection, Output short circuit Protection, CS resistor open/short circuit Protection and Under Voltage Lockout on VDD. All protections are self-recovered.

Package Information

Table 6. SOP-7 Mechanical Data

Size / Symbol	Min.(mm)	Typ.(mm)	Max.(mm)	Size / Symbol	Min.(mm)	Typ.(mm)	Max.(mm)
A	—	—	1.75	D	4.70	4.90	5.10
A1	0.10	0.15	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.728（SC）		
b	0.39	—	0.48	h	0.25	—	0.50
b1	0.38	0.41	0.43	L	0.50	—	0.80
c	0.21	—	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0°	—	8°

Figure 5. Package Outline Dimensions



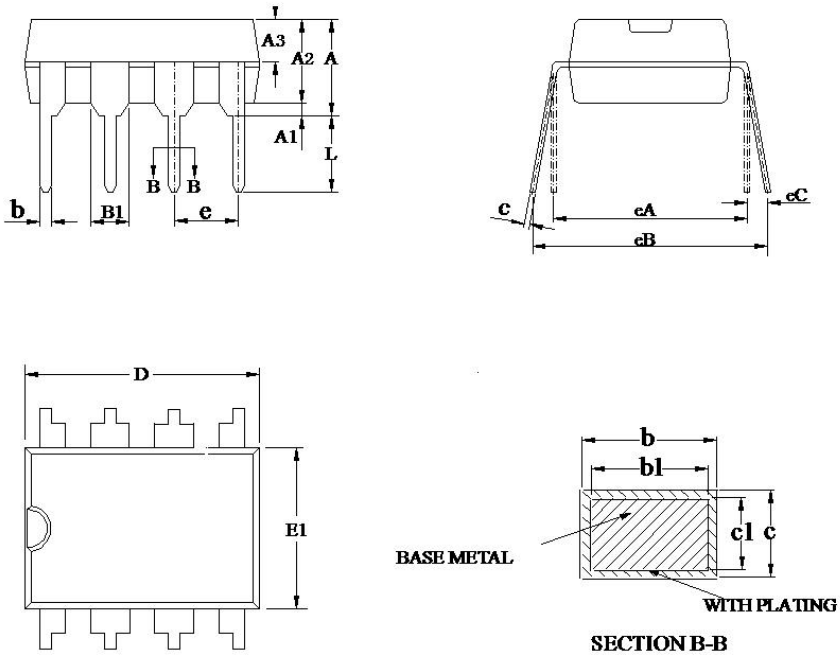
TOP MARK	Package
PN8370 YWWXXXXX	SOP-7

Note: Y: Year Code; WW: Week Code; XXXX: Internal Code

Table 7. DIP-8 mechanical data

Size / symbol	Min.(mm)	Max.(mm)	Size / symbol	Min.(mm)	Max.(mm)
A	3.60	4.00	c1	0.23	0.27
A1	0.51	——	D	9.05	9.45
A2	3.00	3.40	E1	6.15	6.55
A3	1.55	1.65	e	2.54BSC	
b	0.44	0.53	e A	7.62BSC	
b1	0.43	0.48	e B	7.62	9.30
B1	1.52BSC		e C	0.00	0.84
c	0.24	0.32	L	3.00	——

Figure 6. Package Outline Dimensions



TOP MARK	Package
PN8370 YWWXXXXX	DIP-8

Note: Y: Year Code; WW: Week Code; XXXX: Internal Code